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SHAPIRO, LEONID	
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Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

Office Action Summary	**Application No.** 09/994,674	**Applicant(s)** AOKI, TORU	
	Examiner Leonid Shapiro	**Art Unit** 2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _28 January 2004_.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _1-20_ is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _8_ is/are allowed.

6)☒ Claim(s) _1-6 and 11-20_ is/are rejected.

7)☒ Claim(s) _9 and 10_ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _28 January 2004_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

Drawings

1. The drawing was received and approved on 01-28-04. This drawing is Fig.3.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claim 13 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. Limitation of claim 13: " the reference coordinates corresponding to the reference compensation data for R or B being extracted from the reference coordinates corresponding to the reference compensation data for G" is not described in the description.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-6, 11-12 and 18-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. (US Patent No. 6,392,630 B1) in view Konuma et al (JP 11-113019) and Hashimoto et al. (US Patent No. 5,191,455).

As to claim 1, Lin et al. teaches an image data compensation method (See Col. 3, Lines 59-63) to convert image data, indicating gray level of pixels (See Col. 3, Line 63) aligned in a matrix in an X direction and a Y direction into analog data and that compensates the image data when a voltage signal is supplied to each of the pixels (See Figs. 1, 5, items 11-14, 141, 142, 51, in description See from Col. 2, Line 67 to Col. 3, Line 36, and Col. 3, Lines 59-63), Col. 1, Lines 12-28), comprising the steps of; storing reference compensation data for each pair of reference coordinates preset in a display region in which pixels are aligned (See Fig. 1, item 11, in description See Col. 3, Lines 2-11); and storing the first compensation data in association with the each pair of reference coordinates and the levels (See Fig. 1, item 12, in description See Col. 3, Lines 12-14); adding the second compensation data to the image data (See Fig. 1, item 142, in description See Col. 3, Lines 19-30).

Lin et al. do not show storing reference compensation data corresponding to specific levels among levels available to the image data.

Since Lin et al. teaches the compensation process is performed by computing the output signal by adding original 64-level signal and compensation signal (See Figs. 1. 3, items V1, V2, Col. 3, Lines 59-65), it would have been obvious to one of ordinary skill in the art at the time of the invention that storing reference compensation data for each pixel must corresponding to specific levels among levels available to the image data (64) in the Lin et al. method.

Lin et al. do not show an interpolating the stored reference compensation data in the level directions to generate first compensation data corresponding to the levels available to the image data for the each pair of reference coordinates; selectively reading, from the stored first compensation data, pieces of data which correspond to pairs of references coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of image data; interpolating the read first compensation data in the coordinate directions to generate second compensation data corresponding to the image data.

Konuma et al. teaches an interpolation processor (See Drawing 1, item 20, in Detailed Description See page 3, paragraph 0018) that interpolates the reference compensation data stored in memory in the level directions (See Drawings 1, 5, items 42R, 42G, 42G, in Detailed Description See page 7, paragraph 0051) to generate first compensation data corresponding to the levels available to the image data (See Drawing 7, items Z1, Z2, in Detailed Description See page 9, paragraph 0064) for the each pair of reference coordinates (See Drawing 2, items 3, 6, in Detailed Description See page paragraphs 0025-0026); a reading unit that reads selectively, from the first compensation data stored in the compensation table, pieces of data which correspondent to pairs of references coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of image data (See Drawing 2, items 3-4, in Detailed Description See page paragraph 0030); an arithmetic unit that interpolates the read first compensation data in the coordinate directions to generate second compensation data corresponding to the image data (See Drawings 2-4, items 5-7, in Detailed Description See page paragraphs 0041-0043).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement data processing approach as shown by Konuma et al. in the Lin et al. method in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference).

Lin et al. and Konuma et al. do not show a polarity of the voltage signal being inverted based on a predetermined constant potential every predetermined period and adding compensation data to the positive voltage signal and in case in which the voltage signal is negative with respect to the constant potential.

Hashimoto et al. teaches polarity inverting circuit used in compensation of residual voltage (See Fig. 1, item 1, in description See Col. 3, lines 14-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a polarity of the voltage signal being inverted based on a predetermined constant potential every predetermined period and adding compensation data to the positive voltage signal and in case in which the voltage signal is negative with respect to the constant potential as shown by Hashimoto in the Lin et al. and Konuma et al. method in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference) and completely compensate the DC voltage which changes in level (See Col. 4, Lines 21-23 in the Hashimoto et al. reference).

As to claim 2, Lin et al. teaches an image data compensation circuit (See Col. 3, Lines 59-63) to convert image data, indicating gray level of pixels (See Col. 3, Line 63) aligned in a matrix in an X direction and a Y direction into analog data and that compensates the image data when a voltage signal is supplied to each of the pixels (See Figs. 1, 5, items 11-14, 141, 142, 51,

in description See from Col. 2, Line 67 to Col. 3, Line 36, and Col. 3, Lines 59-63), Col. 1, Lines 12-28); a memory that stores reference compensation data for each pair of reference coordinates preset in a display region in which the pixels are aligned (See Fig. 1, item 11, in description See Col. 3, Lines 2-11); a compensation table that stores the first compensation data in association with reference coordinates and the levels (See Fig. 1, item 12, in description See Col. 3, Lines 12-14); an adder that adds the second compensation data to the image data (See Fig. 1, item 142, in description See Col. 3, Lines 19-30).

Lin et al. do not show storing reference compensation data corresponding to specific levels among levels available to the image data.

Since Lin et al. teaches the compensation process is performed by computing the output signal by adding original 64-level signal and compensation signal (See Figs. 1. 3, items V1, V2, Col. 3, Lines 59-65), it would have been obvious to one of ordinary skill in the art at the time of the invention that storing reference compensation data for each pixel must corresponding to specific levels among levels available to the image data (64) in the Lin et al. method.

Lin et al. do not show an interpolation processor that interpolates the reference compensation data stored in memory in the level directions to generate first compensation data corresponding to the levels available to the image data for the each pair of reference coordinates; a reading unit that reads selectively, from the first compensation data stored in the compensation table, pieces of data which correspondent to pairs of references coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of image data; an arithmetic unit that interpolates the read first compensation data in the coordinate directions to generate second compensation data corresponding to the image data.

Konuma et al. teaches an interpolation processor (See Drawing 1, item 20, in Detailed Description See page paragraph 0018) that interpolates the reference compensation data stored in memory (See Drawings 1, 5, items 42R, 42G, 42G, in Detailed Description See page 7, paragraph 0051) to generate first compensation data corresponding to the levels available to the image data (See Drawing 7, items Z1, Z2, in Detailed Description See page 9, paragraph 0064) for the each pair of reference coordinates (See Drawing 2, items 3, 6, in Detailed Description See page paragraphs 0025-0026); a reading unit that reads selectively, from the first compensation data stored in the compensation table, pieces of data which correspondent to pairs of references coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of image data (See Drawing 2, items 3-4, in Detailed Description See page paragraph 0030); an arithmetic unit that interpolates the read first compensation data in the coordinate directions to generate second compensation data corresponding to the image data (See Drawings 2-4, items 5-7, in Detailed Description See page paragraphs 0041-0043).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement data processing approach as shown by Konuma et al. in the Lin et al. apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference).

Lin et al. and Konuma et al. do not show a polarity of the voltage signal being inverted based on a predetermined constant potential every predetermined period and adding compensation data to the positive voltage signal and in case in which the voltage signal is negative with respect to the constant potential.

Hashimoto et al. teaches polarity inverting circuit used in compensation of residual voltage (See Fig. 1, item 1, in description See Col. 3, lines 14-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a polarity of the voltage signal being inverted based on a predetermined cons shown by Hashimoto in the Lin et al. and Konuma et al. apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference) and completely compensate the DC voltage which changes in level (See Col. 4, Lines 21-23 in the Hashimoto et al. reference).

As to claim 18, Lin et al. teaches a liquid crystal display (See Figs. 1, 5, items 11-14, 141, 142, 51, in description See from Col. 2, Line 67 to Col. 3, Line 36 and Col. 1, Lines 12-28), comprising: a memory that stores reference compensation data corresponding to specific levels available to the image data (See Col. 3, Line 63), indicating the gray levels of pixels aligned in the form of matrix in the X direction and the Y direction an image data compensation method (See Col. 3, Lines 59-63) to convert image data, indicating gray level of pixels (See Col. 3, Line 63) aligned in a matrix in an X direction and a Y direction into analog data and that compensates the image data when a voltage signal is supplied to each of the pixels (See Figs. 1, 5, items 11-14, 141, 142, 51, in description See from Col. 2, Line 67 to Col. 3, Line 36, and Col. 3, Lines 59-63), Col. 1, Lines 12-28), for each pair of reference coordinates preset in a display region in which the pixels are aligned (See Fig. 1, item 11, in description See Col. 3, Lines 2-11); a compensation table that stores the first compensation data in association with reference coordinates and the levels (See Fig. 1, item 12, in description See Col. 3, Lines 12-14); an adder that adds the second compensation data to the image data (See Fig. 1, item 142, in description

See Col. 3, Lines 19-30), a d/a converter that converts the compensated image data into analog data (See Fig. 1, item 13, in description See Col. 3, Lines 15-18); a driving circuit that supplies the inverted voltage signal to each of the pixels (See Fig. 1, item 142, in description See Col. 3, Lines 19-30).

Lin et al. do not show an interpolation processor that interpolates the reference compensation data stored in memory in the level directions to generate first compensation data corresponding to the levels available to the image data for the each pair of reference coordinates; a reading unit that reads selectively, from the first compensation data stored in the compensation table, pieces of data which correspondent to pairs of references coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of image data; an arithmetic unit that interpolates the read first compensation data in the coordinate directions to generate second compensation data corresponding to the image data.

Konuma et al. teaches an interpolation processor (See Drawing 1, item 20, in Detailed Description See page paragraph 0018) that interpolates the reference compensation data stored in memory in the level directions to generate first compensation data corresponding to the levels available to the image data for the each pair of reference coordinates (See Drawing 2, items 3, 6, in Detailed Description See page paragraphs 0025-0026); a reading unit that reads selectively, from the first compensation data stored in the compensation table, pieces of data which correspondent to pairs of references coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of image data (See Drawing 2, items 3-4, in Detailed Description See page paragraph 0030); an arithmetic unit that interpolates the read first compensation data in the coordinate directions to generate second

compensation data corresponding to the image data (See Drawings 2-4, items 5-7, in Detailed Description See page paragraphs 0041-0043).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement data processing approach as shown by Konuma et al. in the Lin et al. apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference).

Lin et al. and Konuma et al. do not show a polarity inverter circuit that inverts the polarity of the voltage signal on the basis of the predetermined potential every predetermined period and adding compensation data to the positive voltage signal and in case in which the voltage signal is negative with respect to the constant potential.

Hashimoto et al. teaches polarity inverting circuit used in compensation of residual voltage (See Fig. 1, item 1, in description See Col. 3, lines 14-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a polarity inverter circuit that inverts the polarity of the voltage signal on the basis of the predetermined potential every predetermined period and adding compensation data to the positive voltage signal and in case in which the voltage signal is negative with respect to the constant potential as shown by Hashimoto in the Lin et al. and Konuma et al. apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference) and completely compensate the DC voltage which changes in level (See Col. 4, Lines 21-23 in the Hashimoto et al. reference).

As to claim 3, Hashimoto et al. teaches the adder adding the second compensation data to the image data in only one of the case in which voltage signal is positive and the case in which

the voltage signal is negative; and in the other one of the case in which the voltage signal is positive and the case in which the voltage signal is negative, the adder adding a substantially zero value to the image data (See Figs. 1-3, items 1, 2, in description See Col. 3, Lines 20-64).

As to claim 4, Lin et al. teaches the reference compensation data corresponding to the specific level being a value adjusted so as reduce the difference in the gray level between the one case I which the sum of the reference compensation data and the image data corresponding to the specific level is applied to a pixel electrode and the other case in which the reference compensation data is not added to the image data corresponding to the specific level and the image data is applied to the pixel electrode (see fig. 1, items 11. 141-142, in description se from Col. 3, Line 59 to col. 4, Line 7).

As to claim 5, Konuma teaches the reading unit with; an X counter that counts first clock signals which used as a time reference for X-direction scanning in the display region and that generates X-coordinate data including the X coordinate of the pixel corresponding to the image data in the display region; an Y counter that counts first clock signals which used as a time reference for Y-direction scanning in the display region and that generates Y-coordinate data including the Y coordinate of the pixel corresponding to the image data in the display region (See Drawing 2, item 2, in Detailed Description See paragraph 0023); an address generator that specifies a plurality of pairs of reference coordinates positioned near coordinates of the pixel corresponding to the image data based on the X-coordinate data and Y-coordinate data and generates addresses to read the corresponding first compensation data from the compensation table based on specified pair of reference coordinates and the level of the image data (See Drawing 2, items 3, 6, in Detailed Description See paragraph 0023-0025); the arithmetic unit

performing interpolation in accordance with the distance from the coordinates of the image data specified by X-coordinate and Y-coordinate data to (See Drawing 2, items 5-7, in Detailed Description See paragraph 0041).

As to claim 6, 11, Konuma et al. teaches the memory, interpolation processor, X-Y counter being shared among RGB being shared among RGB colors (See Drawing 2, items 3-7), Lin et al. teaches the adder being provided in association with each of the RGB colors (see Fig. Item 142).

Lin et al. Konuma et al. and Hashimoto et al. do not show the compensation table, the arithmetic unit, the address generator being provided in association with each of the RGB colors.

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the compensation table, the arithmetic unit, the address generator being provided in association with each of the RGB colors or any other combination in the Lin et al., Konuma et al. and Hashimoto apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference).

As to claim 19, Lin et al. teaches a liquid crystal display (See Fig. 1, in description See Col. 2, Lines 66-67).

4. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al., Konuma et al. and Hashimoto et al. as applied to claim 2 above, and further in view of Miyashita et al. (US Patent No. 6,115,084).

Lin et al., Konuma et al. and Hashimoto et al. do not show specific levels to which the reference compensation data correspond including first and second levels corresponding to first and second points at which a display characteristic curve indicating at least one of transmissivity

and reflectivity with respect to the effective value of the voltage applied to the liquid crystal capacitor suddenly changes and at least one level between the first and second level.

Miyashita et al. teaches show specific levels to which the reference compensation data correspond including first and second levels corresponding to first and second points at which a display characteristic curve indicating at least one of transmissivity and reflectivity with respect to the effective value of the voltage applied to the liquid crystal capacitor suddenly changes and at least one level between the first and second (See Fig. 29, items G2, G14 and Gn, in description See Col. 2, Lines 1-10).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use specific three specific levels as shown by Miyashita et al. in the Lin et al., Konuma et al. and Hashimoto apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference).

5. Claims 12, 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view of Konuma et al., Hashimoto et al. and Iwama et al. (US Patent No. 6,177,914 B1).

As to claim 12, Lin et al., Konuma et al. and Hashimoto et al. do not show the memory storing a greater amount of reference compensation data for G than for R or for B.

Iwama et al. teaches that the compensation coefficient be precisely calculated for the green color since human visual sensitivity is more sensitive to changes in green color (See Col. 7, Lines 29-50).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use more a greater amount of reference compensation data for G than for R or for B as shown

by Iwama et al. in Lin et al., Konuma et al. and Hashimoto et al. apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference).

As to claim 20, Lin et al. teaches an image data compensation circuit (See Col. 3, Lines 59-63) to convert image data, indicating gray level of pixels (See Col. 3, Line 63) aligned in a matrix in an X direction and a Y direction into analog data and that compensates the image data when a voltage signal is supplied to each of the pixels (See Figs. 1, 5, items 11-14, 141, 142, 51, in description See from Col. 2, Line 67 to Col. 3, Line 36, and Col. 3, Lines 59-63), Col. 1, Lines 12-28); a memory that stores reference compensation data for each pair of reference coordinates preset in a display region in which the pixels are aligned (See Fig. 1, item 11, in description See Col. 3, Lines 2-11); a compensation table that stores the first compensation data in association with reference coordinates and the levels (See Fig. 1, item 12, in description See Col. 3, Lines 12-14); an adder that adds the second compensation data to the image data (See Fig. 1, item 142, in description See Col. 3, Lines 19-30).

Lin et al. do not show storing reference compensation data corresponding to specific levels among levels available to the image data.

Since Lin et al. teaches the compensation process is performed by computing the output signal by adding original 64-level signal and compensation signal (See Figs. 1. 3, items V1, V2, Col. 3, Lines 59-65), it would have been obvious to one of ordinary skill in the art at the time of the invention that storing reference compensation data for each pixel must corresponding to specific levels among levels available to the image data (64) in the Lin et al. method.

Lin et al. do not show an interpolation processor that interpolates the reference compensation data stored in memory in the level directions to generate first compensation data corresponding to the levels available to the image data for the each pair of reference coordinates; a reading unit that reads selectively, from the first compensation data stored in the compensation table, pieces of data which correspondent to pairs of references coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of image data; an arithmetic unit that interpolates the read first compensation data in the coordinate directions to generate second compensation data corresponding to the image data.

Konuma et al. teaches an interpolation processor (See Drawing 1, item 20, in Detailed Description See page paragraph 0018) that interpolates the reference compensation data stored in memory (See Drawings 1, 5, items 42R, 42G, 42G, in Detailed Description See page 7, paragraph 0051) to generate first compensation data corresponding to the levels available to the image data (See Drawing 7, items Z1, Z2, in Detailed Description See page 9, paragraph 0064) for the each pair of reference coordinates (See Drawing 2, items 3, 6, in Detailed Description See page paragraphs 0025-0026); a reading unit that reads selectively, from the first compensation data stored in the compensation table, pieces of data which correspondent to pairs of references coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of image data (See Drawing 2, items 3-4, in Detailed Description See page paragraph 0030); an arithmetic unit that interpolates the read first compensation data in the coordinate directions to generate second compensation data corresponding to the image data (See Drawings 2-4, items 5-7, in Detailed Description See page paragraphs 0041-0043).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement data processing approach as shown by Konuma et al. in the Lin et al. apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference).

Lin et al. and Konuma et al. do not show a polarity of the voltage signal being inverted based on a predetermined constant potential every predetermined period and adding compensation data to the positive voltage signal and in case in which the voltage signal is negative with respect to the constant potential.

Hashimoto et al. teaches polarity inverting circuit used in compensation of residual voltage (See Fig. 1, item 1, in description See Col. 3, lines 14-24).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a polarity of the voltage signal being inverted based on a predetermined cons shown by Hashimoto in the Lin et al. and Konuma et al. apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference) and completely compensate the DC voltage which changes in level (See Col. 4, Lines 21-23 in the Hashimoto et al. reference).

Lin et al., Konuma et al. and Hashimoto et al. do not show the memory that stores reference coordinates numbering fewer that a number of pixels in the matrix of the display, the reference compensation data being stored for each of RGB colors, the reference compensation data for G color being stored in correspondence with more pairs of reference coordinates than reference compensation data for color or for B color, the reference compensation data for each of

RGB colors including reference compensation data for a number of specific levels that is smaller than a number of levels available for the image data.

Iwama et al. teaches that the compensation coefficient be precisely calculated for the green color since human visual sensitivity is more sensitive to changes in green color (See Col. 7, Lines 29-50).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use a greater amount of reference compensation data for G than for R or for B as shown by Iwama et al. in Lin et al., Konuma et al. and Hashimoto et al. apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference).

6. Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lin et al. in view Konuma et al. and further in view of Sekizawa et al. (US Patent No. 4,663,662).

As to claim 14, Lin et al. teaches an image data compensation circuit (See Col. 3, Lines 59-63) to convert image data, indicating gray level of pixels (See Col. 3, Line 63) aligned in a matrix in an X direction and a Y direction into analog data and that compensates the image data when a voltage signal is supplied to each of the pixels (See Figs. 1, 5, items 11-14, 141, 142, 51, in description See from Col. 2, Line 67 to Col. 3, Line 36, and Col. 3, Lines 59-63), Col. 1, Lines 12-28); a memory that stores reference compensation data (See Fig. 1, item 11, in description See Col. 3, Lines 2-11); an adder that adds the second compensation data to the image data (See Fig. 1, item 142, in description See Col. 3, Lines 19-30).

Lin et al. does not show a first compensation data generator that interpolates the reference compensation data stored in memory in the level directions based on half tone image data of the image data in one polarity and for generating first compensation data, a second compensation data generator that interpolates coordinate data for half tone image and the first compensation data in the coordinate directions and for generating second compensation data.

Konuma et al. teaches an interpolation processor (See Drawing 1, item 20, in Detailed Description See page paragraph 0018) that interpolates the reference compensation data stored in memory in the level directions to generate first compensation data corresponding to the levels available to the image data for the each pair of reference coordinates (See Drawing 2, items 3, 6, in Detailed Description See page paragraphs 0025-0026); a reading unit that reads selectively, from the first compensation data stored in the compensation table, pieces of data which correspondent to pairs of references coordinates positioned near the coordinates of the pixel corresponding to the image data and which correspond to the level of image data (See Drawing 2, items 3-4, in Detailed Description See page paragraph 0030); an arithmetic unit that interpolates the read first compensation data in the coordinate directions to generate second compensation data corresponding to the image data (See Drawings 2-4, items 5-7, in Detailed Description See page paragraphs 0041-0043).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement data processing approach as shown by Konuma et al. in the Lin et al. apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Abstract in the Konuma reference).

Lin et al. and Konuma et al. do not show a memory that stores white reference level, black reference level, and at least one piece of intermediate reference compensation data.

Sekizawa et al. teaches storing in memory white and black reference signals (See Fig. 13, items Iw, Ib, 141, 145, in description See col. 9, Lines 15-37).

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement a polarity of the voltage signal being inverted based on a predetermined cons shown by Sekizawa in the Lin et al. and Konuma et al. apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Problem To Be Solved in the Konuma reference).

As to claim 15, Sekizawa et al. teaches to store white and black levels in the memory (See Fig. 13, items Iw, Ib, 141, 145, in description See col. 9, Lines 15-37) and Lin et al. teaches a memory device would be used as first compensation data (See Fig. 1, items 11-12).

As to claim 16, Sekizawa et al. teaches to store white and black levels in the memory (See Fig. 13, items Iw, Ib, 141, 145, in description See col. 9, Lines 15-37).

Lin et al., Konuma et al. and Sekizawa et al. do not show the first compensation data generator using the product of the white reference compensation data or the black reference compensation data in the memory and coefficient in accordance with difference between the image data at the white or black reference level or the black reference level and the white reference compensation data or the black reference compensation data in the memory as the first compensation data.

It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the first compensation data generator using the product of the white reference

compensation data or the black reference compensation data in the memory and coefficient in accordance with difference between the image data at the white or black reference level or the black reference level and the white reference compensation data or the black reference compensation data in the memory as the first compensation data in the Lin et al., Konuma et al. and Sekizawa apparatus in order to correct luminance and chrominance unevenness caused in a valid screen (See Problem To Be Solved in the Konuma reference).

As to claim 17, Hashimoto et al. teaches the intermediate reference compensation data in memory being computed based on a deficiency or an excess of luminance level in positive polarity and negative polarity in a region generated by dividing a screen (See Figs. 1-3, items 1, 2, in description See Col. 3, Lines 20-64).

Allowable Subject Matter

7. Claims 8-10 are allowed.

8. The following is a statement of reasons for the indication of allowable subject matter: Relative to independent claim 8, the major difference between the teaching of the prior art of record (US patent No. 6,392,630 B1 to Lin et al., JP 5,852,428 to Konuma et al. and US Patent No. 5,191,455 to Hashimoto et al.) and the instant invention is that the said prior art **does not teach** interpolation for reference compensation data related levels below, between and exceeding first and second level.

Response to Arguments

9. Applicant's arguments filed 01-28-04 have been fully considered but they are not persuasive:

On page 14, 2nd and 3rd paragraphs, Applicant's stated in relation to claims 1-2, that none of references teaches storing reference compensation data corresponding to specific levels and Lin discloses the memory for storing the compensation signals for each pixels. However, the compensation process is performed by computing the output signal by adding original 64-level signal and compensation signal (See Figs. 1. 3, items V1, V2, Col. 3, Lines 59-65 in the Lin reference) and one of ordinary skill in the art at the time of the invention will recognize that stored compensation signal also has to be corresponding to 64 specific levels.

On page 14, 4th paragraph, Applicant's stated in relation to claims 1-2, that none of references teaches the stored reference in the level directions. However, Konuma teaches the reference compensation data stored in memory in the level directions (See Drawings 1, 5, items 42R, 42G, 42G, in Detailed Description See page 7, paragraph 0051) to generate first compensation data corresponding to the levels available to the image data (See Drawing 7, items Z1, Z2, in Detailed Description See page 9, paragraph 0064).

On page 14, last paragraph and page 15, second paragraph, Applicant's stated in relation to claims 1-2, that there is no advantage be obtained by modifying Lin's compensation circuit to use the interpolating processing section of Konuma. However, an interpolating process will add compensation in the level directions to the hardware of Lin.

On page 14, 3rd paragraph, Applicant's stated in relation to claims 1-2, that Office has engaged in classic hindsight reconstruction of the references. However, in response to

applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning, it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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VIJAY SHANKAR
PRIMARY EXAMINER